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10/652,135	08/29/2003	Philip E. May	CML00769D	1155

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LEVEQUE INTELLECTUAL PROPERTY LAW, P.C.
221 EAST CHURCH ST.
FREDERICK, MD 21701

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/652,135	MAY ET AL.	
	Examiner	Art Unit	
	Tonia LM Dollinger	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/19/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendment filed September 12, 2007 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

a. "In general, a loop comprises a prolog, a loop-body and an epilog. The prolog and epilog instructions are generally a subset of the instructions in the ~~body of the~~ loop. The prolog instructions are placed at the start of the loop, before the loop body and are used for priming the pipeline. The epilog instructions are placed at the end of the loop, after the loop body and are used for draining the pipeline. According to the present invention, mechanisms are provided to guard the execution (committing of results) to the correct subset of the loop-body. Consequently, the data path can repeatedly execute the loop-body, thereby eliminating the prolog and epilog code."

2. Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 13-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claims contain prolog and epilog instructions. The specification has newly defined prolog and epilog. This new meaning of the claims was not properly disclosed in the original application and it is not clear whether Applicant's had possession of the invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 13-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Referring to claim 13, the limitation "a...loop having a loop body but no prolog instructions" is unclear. According to applicant's specification, paragraph [0003], instructions at the start of the loop are described as the prolog instructions. It is not understood how a loop can have no instructions at the start of the loop. Each loop must have instruction(s) at the start of the loop otherwise the loop would contain no instructions and it wouldn't actually be a loop. It would be nothing. Appropriate correction is required. For the purposes of examination this limitation is interpreted as "the loop body instructions enter a pipeline with instruction(s) already executing in the pipeline stages".

8. Claims 14-19 are rejected for incorporating the defects of claim 13.

9. Referring to claim 19, the limitation "wherein the loop has not epilog instructions" is unclear. According to applicant's specification, paragraph [0003], instructions at the end of the loop are described as the epilog instructions. It is not understood how a loop can have no instructions at the end of the loop. Each loop must have instruction(s) at the end of the loop otherwise the loop would contain no instructions and it wouldn't actually be a loop. It would be nothing. Appropriate correction is required. Appropriate correction is required. For the purposes of examination this limitation is interpreted as "the loop body instructions exit a pipeline with instructions following the loop executing in the pipeline stages".

10. Referring to claim 20, the limitation "a...loop having a loop body but no epilog instructions" is unclear. According to applicant's specification, paragraph [0003], instructions at the end of the loop are described as the epilog instructions. It is not understood how a loop can have no instructions at the end of the loop. Each loop must have instruction(s) at the end of the loop otherwise the loop would contain no instructions and it wouldn't actually be a loop. It would be nothing. Appropriate correction is required. Appropriate correction is required. For the purposes of examination this limitation is interpreted as "the loop body instructions exit a pipeline with instructions following the loop executing in the pipeline stages".

11. Claims 21-24 are rejected for incorporating the defects of claim 20.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 13-16 and 19-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hennessy and Patterson, Computer Architecture A Quantative Approach, 1996, Morgan Kaufman Publishers, Inc., Second Edition, pages 239-247 (hereinafter referred to as Hennessy).

14. Referring to claim 13, Hennessy has taught a method for executing a pipelined program loop having a loop body but no prolog instructions on a processor (This limitation is interpreted as "the loop body instructions enter a pipeline with instruction(s) already executing in the pipeline stages" (see the 112 rejection above). page 240, The loop enters the pipeline with at least one instruction executing in the pipeline, A[1] = A[1] + B[1];), the processor comprising a plurality of functional units coupled through an interconnection switch and controlled by a controller (pages 246 and 247, at least the multiply unit, integer unit, add unit and divide unit are the functional units), each functional unit of the plurality of functional units having at least one input for receiving an input data value and an associated input data validity tag (pages 246 and 247, Fj, Fk are the source registers that are input to the functional units from functional units Qj and Qk. Rj, Rk and register result status is the validity of the input data.) the method comprising: executing the loop body for a plurality of iterations (page 240, iterations of the loop); and at each iteration of a plurality of iterations: determining if the input data values are valid by checking the associated input data validity tags (page 246 and 247,

register result status, Rj and Rk, The scoreboard is checked for each instruction to ensure all data values are valid before executing the instructions.).

15. Referring to claim 14, Hennessy has taught a method in accordance with claim 13, as described above, and wherein a functional unit of the plurality of functional units includes a result register for storing an intermediate result (page 246 and 247, When Fj or Fk are dependent on a prior operation.) and an associated output data validity tag (page 246 and 247, register result status, Rj and Rk indicate the readiness of operands dependent on other operations executed and output from the various functional units.), the method further comprising: at each iteration of the plurality of iterations: if all of the input data values are valid, performing a functional operation on the input data values (page 246 and 247, When the flags of a functional unit indicate that all data values are ready, then the functional unit performs it operation on the input values.), storing the result of the functional operation in the result register and setting the associated output data validity tag to indicate that the intermediate result is valid (page 246 and 247, For example-F2 in the multiply is dependent on F2 in the prior load. When the load is finished executing and the result is available, then the tag on the multiply instruction indicates that the intermediate result from the load instruction is ready.); and if any of the input data values is invalid, setting the associated output data validity tag to indicate that the intermediate result is invalid (page 246 and 247, register result status , Rj and Rk are set to indicate the validity of a functional units input data that is output from the various functional units.).

16. Referring to claim 15, Hennessy has taught a method in accordance with claim 14, as described above, and further comprising initializing an output data validity tag in the result register of each of the plurality of functional units to indicate that the associated intermediate result is invalid (page 246 and 247, Rj and Rk are set to NO and register result status is listed as pending.).

17. Referring to claim 16, Hennessy has taught a method in accordance with claim 15, as described above, and further comprising: storing output data values only if the associated output data validity tag indicates that the data is valid (page 246 and 247, An operation is performed and the data is output only if the validity tags indicate that the data is valid.).

18. Referring to claim 19, Hennessy has taught a method in accordance with claim 15, as described above, and wherein the pipelined program loop has no epilog instructions (This limitation is interpreted as "the loop body instructions exit a pipeline with instructions following the loop executing in the pipeline stages" (see the 112 rejection above). page 240, The loop exits the pipeline with at least one instruction following the loop in the pipeline, B[101] = C[100] + D[100];) and the processor further comprises at least one data sink (pages 246-247, Fi), each data sink being associated with a sink iteration counter (page 240, i) and operable to receive an output data value and an associated output data validity tag from the interconnection switch (page 246 and 247, Rj and Rk indicate the readiness of operands dependent on other operations executed and output from the various functional units. Also see register result status), the method further comprising: initializing the sink iteration counter of each data sink

(page 240, "i" is initialized to 1); and at each iteration of the specified number of iterations: determining the validity of the output data from the associated output data validity tag (page 240, page 246 and 247, Rj and Rk indicate the readiness of operands dependent on other operations executed and output from the various functional units. The validity of dependent instructions in a loop are checked each iteration. Also see register result status.); if the output data is valid: determining from the sink iteration counter if all data values have been committed to memory (page 240, When a dependent loop instruction executes, the iteration counter is checked before the loop executes again.); adjusting the sink iteration counter associated with the data sink unit if not all data values have been committed to memory (page 240, I is incremented each cycle until all of the data values in the loop are committed to memory.); committing the output data value to memory if not all data values have been committed to memory (page 240, Data values are committed to memory during loop execution.); and signaling the controller if all data values have been committed to memory (page 240, the controller is signaled to stop executing the loop when I is greater than 99.).

19. Referring to claim 20, Hennessy has taught a method for executing a pipelined program loop having a loop body but no epilog instructions on a processor (This limitation is interpreted as "the loop body instructions exit a pipeline with instructions following the loop executing in the pipeline stages" (see the 112 rejection above). page 240, The loop exits the pipeline with at least one instruction following the loop in the pipeline, B[101] = C[100] + D[100];) comprising a plurality of functional units (pages 246 and 247, at least the multiply unit, integer unit, add unit and divide unit are the functional

units) and at least one data sink coupled through an interconnection switch and controlled by a controller (pages 246-247, ·Fi), each data sink being associated with a sink iteration counter (page 240, "i" is a source iteration counter.), the method comprising: initializing each sink iteration counter (page 240, "i" is initialized to 1.); executing the loop body for a specified number of iterations (page 240, executed I, or 99, times.); and at each iteration of the specified number of iterations for which a data value is to be sunk by a data sink unit: determining if the sink iteration counter indicates that all data values have been committed to memory (page 240, "i" is checked each iteration to determine if all of the iterations have been executed, or if all data values in the loop have been committed to memory.).

20. Referring to claim 21, Hennessy has taught a method in accordance with claim 20, as described above, and further comprising committing the data value to memory if not all data values have been committed to memory (page 240, when "i" is 1 to 99, then all instructions in the loop are executed and their data values are committed to memory.).

21. Referring to claim 22, Hennessy has taught a method in accordance with claim 20, as described above, and further comprising adjusting the sink iteration counter associated with the data sink unit if not all data values have been committed to memory (page 240, "i" is incremented until the end of the loop, which is when all data values have been committed to memory.).

22. Referring to claim 23, Hennessy has taught a method as in claim 20, as described above, and further comprising each data sink unit signaling the controller

when the associated sink iteration counter indicates that all data values have been committed to memory (page 240, When "i" is incremented to 100, then all data values have been committed to memory and the controller proceeds to execute the instructions following the loop.).

23. Referring to claim 24, Hennessy has taught a method as in claim 23, as described above, and further comprising terminating the execution of the pipelined program loop after all data sink units have signaled to the controller that all their data values have been committed to memory (page 240, When "i" is incremented to 100, then all data values have been committed to memory and the execution of the loop is terminated. The controller then proceeds to execute the instructions following the loop.).

Response to Arguments

24. Applicant's arguments filed September 12, 2007 with respect to claims 13-16 and 19-24 have been fully considered but they are not persuasive.

25. On pages 10 and 11, Applicant argues in essence:

> *"Claims 13-24 have been rejected under 35 USC §112 as being indefinite. Applicant respectfully traverses this rejection of the claims in view of the amendment to specification on page 6, lines 1-5."*

However, the amendment to the specification is objected to for containing new subject matter. Without this background knowledge in the specification, the claims are still unclear.

26. In response to applicant's argument on page 11, lines 14-28, page 12, lines 17-18 and page 14, lines 4-32 that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the prolog is one or more instructions at the start of the loop used for priming the pipeline, while the epilog is one or more instructions at the end of the loop that are used for draining the pipeline and a scoreboard that eliminates prolog instructions) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

27. On pages 11 and 12, Applicant argues in essence:

> *"A further element of claim 13 is "determining if the input data values are valid by checking the associated input data validity tags." This element is not disclosed by the Hennessy reference. The examiner refers to the scoreboard on page 247 of the Hennessy reference. However, the score board relates to instruction status not data validity. Each entry in the scoreboard corresponds to an instruction or to a function unit executing an instruction. There are no entries that relate to data validity."*

However, the entries in Hennessy do relate to data validity. As shown on page 247, when a register is not valid for reading, then the register result status will indicate as such. The register result status indicates when the register value is pending and not valid (i.e. not logically correct to use at that time). Therefore this argument is moot.

28. On page 12, Applicant argues in essence:

> *"The entries in the scoreboard are not associated with the data..."*

However, as shown on page 247, the scoreboard is concerned with the data. In particular the scoreboard tracks when the result data is available, or when it is valid to read the data. So the scoreboard is associated with the data. Therefore this argument is moot.

29. On pages 12 and 13, Applicant argues in essence:

"The scoreboard of the Hennessy shows if an instruction has been completed and the results are ready, but does not indicate whether the result valid or invalid. For example, the result of an operation is invalid if any of the input operands is invalid. ... Hennessy does not disclose a method for tracking data validity."

However, the definition of valid is "logically correct." When the register result status indicates that a register is pending and not available, then it is not logically correct to use the data for other instructions at this time, i.e. the data is invalid. The data will become logically correct to use when the register result status indicates that the data is not pending and therefore the data is valid. So the register result status of Hennessy indicates and tracks whether the data is valid or not. Therefore this argument is moot.

Allowable Subject Matter

30. A prior art rejection has NOT been made with respect to claims 17 and 18.

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia LM Dollinger whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLMD

Tonia L. M. Dollinger
Primary Examiner
December 7, 2007